FAIRCHILD SEMICONDUCTOR®

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74VHC573
Octal D-Type Latch with 3-STATE Outputs

General Description

The VHC573 is an advanced high speed CMOS octal latch with 3-STATE output fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. This 8-bit D-type latch is controlled by a latch enable input (LE) and an Output Enable input ($\overline{OE}$). When the $\overline{OE}$ input is HIGH, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

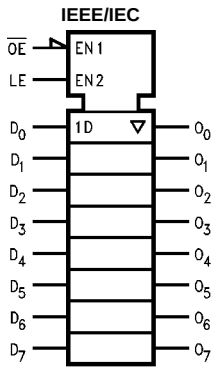
- High Speed: t_{PD} = 5.0 ns (typ) at V_{CC} = 5V
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min)
- Power Down Protection is provided on all inputs
- Low Noise: V_{OLP} = 0.6V (typ)
- Low Power Dissipation: I_{CC} = 4 μA (Max) @ T_A = 25°C
- Pin and function compatible with 74HC573

Ordering Code:

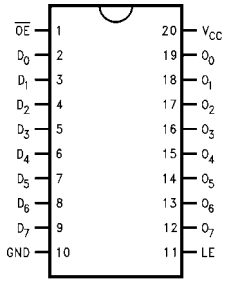
Order Number	Package Number	Package Description
74VHC573M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VHC573SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC573MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC573N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	3-STATE Output Enable Input
O_0–O_7	3-STATE Outputs

Functional Description

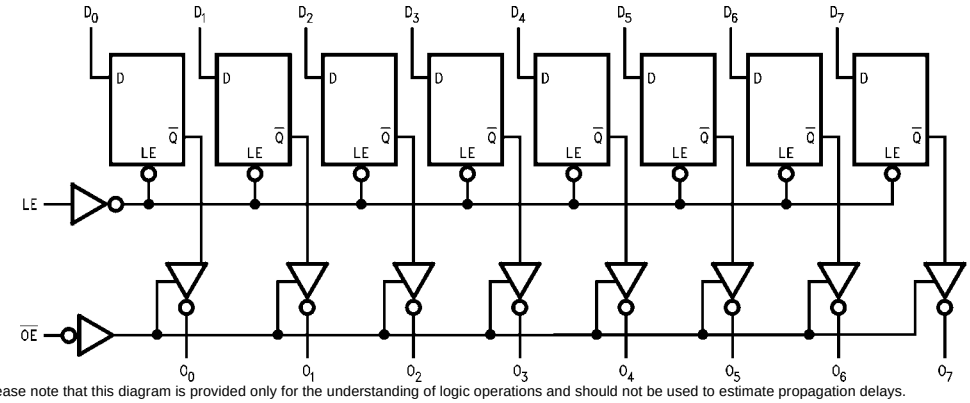
The VHC573 contains eight D-type latches with 3-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs, a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode, but, this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ± 0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ± 0.5V	0 ~ 20 ns/V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input	2.0	1.50			1.50		V		
	Voltage	3.0 – 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Input	2.0			0.50		0.50	V		
	Voltage	3.0 – 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level Output	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH}	
	Voltage	3.0	2.9	3.0		2.9			or V_{IL}	I_{OH} = −50 μA
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	LOW Level Output	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH}	
	Voltage	3.0		0.0	0.1		0.1		or V_{IL}	I_{OL} = 50 μA
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{OZ}	3-STATE Output	5.5			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL}	
	Off-State Current								V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	0 – 5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C		Units	Conditions
			Typ	Limits		
V_{OLP} (Note 3)	Quiet Output Maximum Dynamic V_{OL}	5.0	0.9	1.2	V	C_L = 50 pF
V_{OLV} (Note 3)	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.8	−1.0	V	C_L = 50 pF
V_{IHD} (Note 3)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	C_L = 50 pF
V_{ILD} (Note 3)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	C_L = 50 pF

Note 3: Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
t_{PLH}	Propagation Delay	3.3 ± 0.3		7.6	11.9	1.0	14.0	ns		C_L = 15 pF
t_{PHL}	Time (LE to O_n)			10.1	15.4	1.0	17.5			C_L = 50 pF
		5.0 ± 0.5		5.0	7.7	1.0	9.0	ns		C_L = 15 pF
				6.5	9.7	1.0	11.0			C_L = 50 pF
t_{PLH}	Propagation Delay	3.3 ± 0.3		7.0	11.0	1.0	13.0			C_L = 15 pF
t_{PHL}	Time ($D–O_n$)			9.5	14.5	1.0	16.5	ns		C_L = 50 pF
		5.0 ± 0.5		4.5	6.8	1.0	8.0			C_L = 15 pF
				6.0	8.8	1.0	10.0			C_L = 50 pF
t_{PZL}	3-STATE Output	3.3 ± 0.3		7.3	11.5	1.0	13.5	ns	R_L = 1 kΩ	C_L = 15 pF
t_{PZH}	Enable Time			9.8	15.0	1.0	17.0			C_L = 50 pF
		5.0 ± 0.5		5.2	7.7	1.0	9.0	ns		C_L = 15 pF
				6.7	9.7	1.0	11.0			C_L = 50 pF
t_{PLZ}	3-STATE Output	3.3 ± 0.3		10.7	14.5	1.0	16.5	ns	R_L = 1 kΩ	C_L = 50 pF
t_{PHZ}	Disable Time	5.0 ± 0.5		6.7	9.7	1.0	11.0			C_L = 50 pF
t_{OSLH}	Output to Output Skew	3.3 ± 0.3			1.5		1.5	ns	(Note 4)	C_L = 50 pF
t_{OSHL}		5.0 ± 0.5			1.0		1.0			C_L = 50 pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open	
C_{OUT}	Output Capacitance			6				pF	V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance			29				pF	(Note 5)	

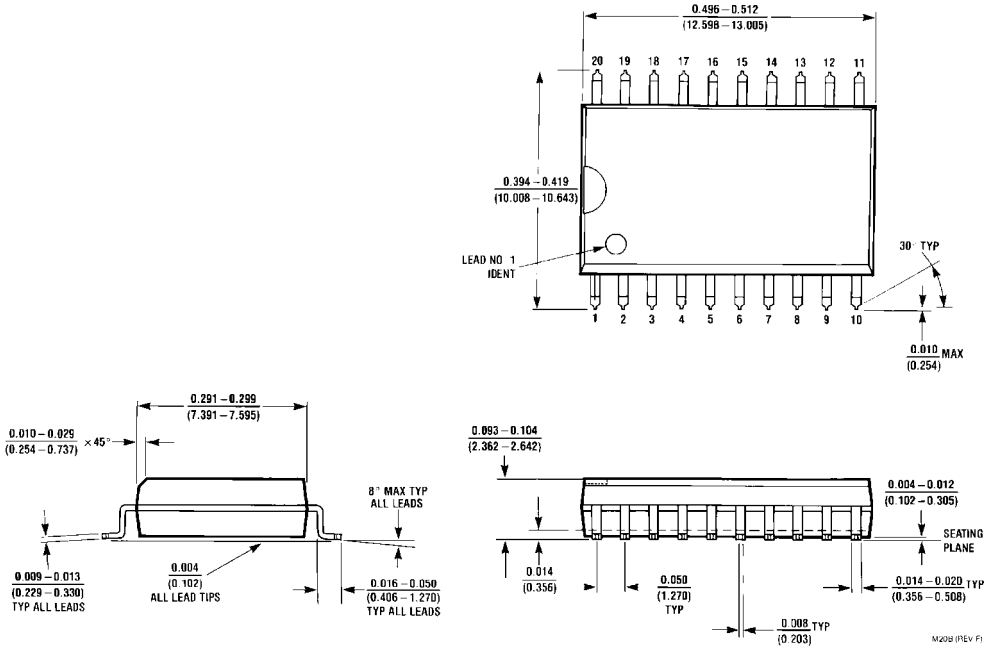
Note 4: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH\ max} - t_{PLH\ min}|$; $t_{OSHL} = |t_{PHL\ max} - t_{PHL\ min}|$

Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = $C_{PD} * V_{CC} * f_{IN} + I_{CC}/8$ (per Latch). The total C_{PD} when n pcs. of the Latch operates can be calculated by the equation: C_{PD}(total) = 21 + 8n.

AC Operating Requirements

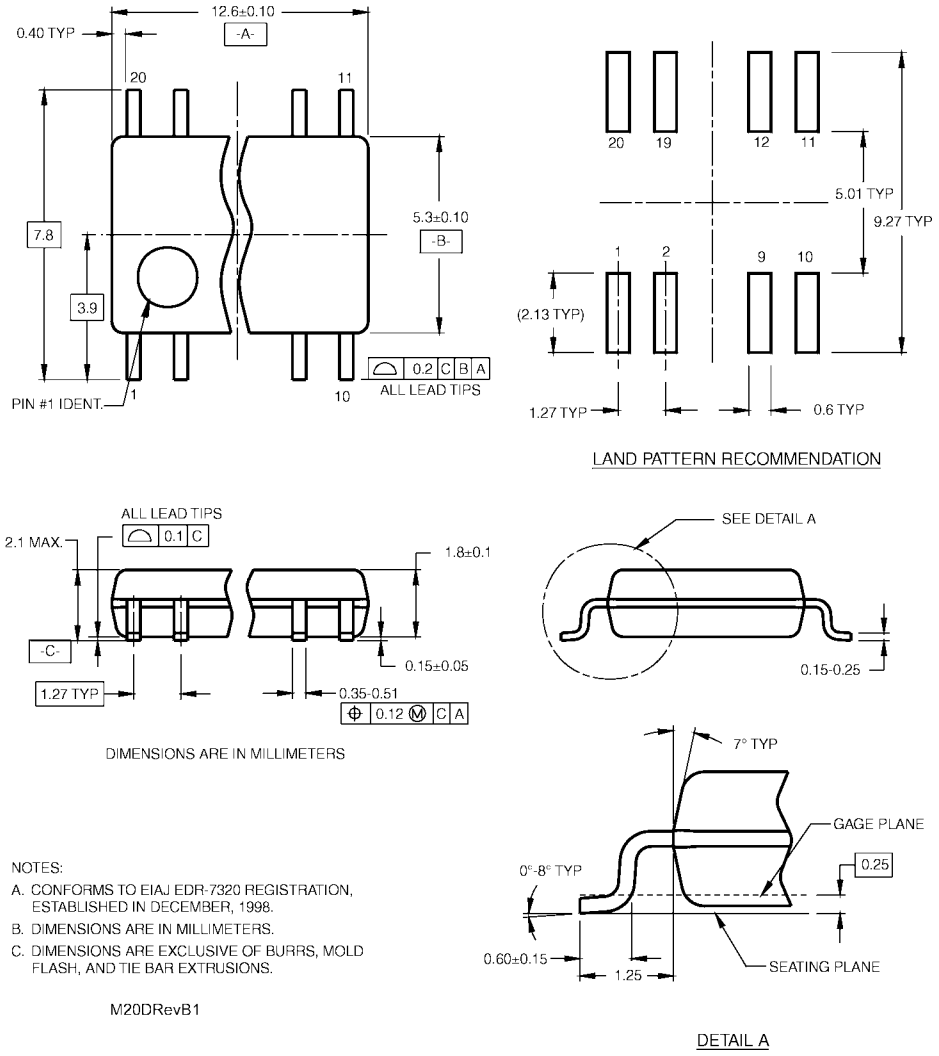
Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units
			Min	Typ	Max	Min	Max	
t_w(H)	Minimum Pulse	3.3 ± 0.3	5.0			5.0		ns
t_w(L)	Width (LE)	5.0 ± 0.5	5.0			5.0		
t_S	Minimum Setup Time	3.3 ± 0.3	3.5			3.5		ns
		5.0 ± 0.5	3.5			3.5		
t_H	Minimum Hold Time	3.3 ± 0.3	1.5			1.5		ns
		5.0 ± 0.5	1.5			1.5		

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

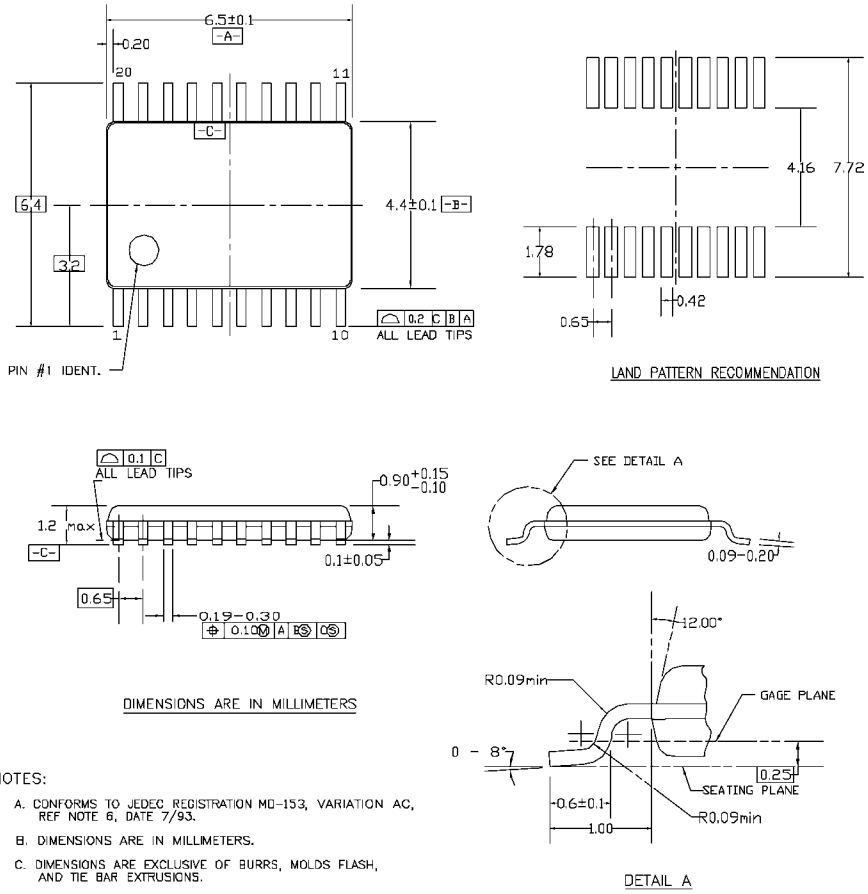
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

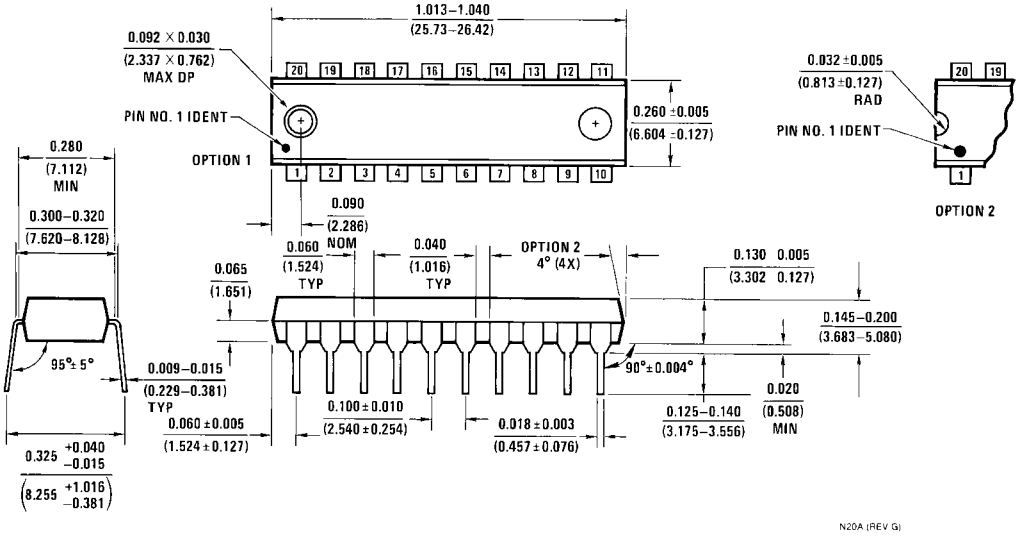
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A